WHAT IS CLAIMED IS:

1. An ATM switch which includes at least one basic switch, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

2. An ATM switch which includes a first stage, a second stage and a third stage each of which stages includes at least one basic switch, wherein said first stage, said second stage and said third stage are connected, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

3. The ATM switch as claimed in claim 1, said means comprising:

a cross-point at which an input line and an output line are crossed;

a first buffer which stores a cell arriving from said input line;

a second buffer which stores a cell arriving from a cross-point; and

means which compares time information of a head cell in said first buffer with time information

of a head cell in said second buffer and sends a head cell with earlier time information to a cross-point or said output port.

4. The ATM switch as claimed in claim 3, wherein said input lines are classified into a plurality of groups,

said first buffer storing cells arriving from said input lines of one of said groups;

time information of a cell with the earliest time information among cells in said first buffer being compared with time information of said head cell in said second buffer, and

a cell with earlier time information being sent to a cross-point or said output port.

5. The ATM switch as claimed in claim 1, further comprising adding means which adds arriving time information to an arriving cell as said time information.

6. The ATM switch as claimed in claim 5, wherein said adding means generates a dummy cell and adds time information to said dummy cell if there is no input cell.

7. The ATM switch as claimed in claim 6, wherein said basic switch transfers said dummy cells or said arriving cells with said time information to output ports other than the destination of said arriving cell.

8. The ATM switch as claimed in claim 7, wherein said basic switch allows said dummy cell to be overwritten by an arriving cell.

9. The ATM switch as claimed in claim 5,

wherein said time information is a value repeating periodically;

said adding means adding a flag for identifying said period to said cell, and

said basic switch identifying said period by referring to said flag.

10. The ATM switch as claimed in claim 1, wherein said basic switch includes a delay time counter, adds said delay time, and uses said added delay time as said time information.

11. A large-sized ATM switch which

includes interconnected ATM switches each of which ATM switches includes at least one basic switch, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

12. An ATM switch which includes at least one basic switch, said basic switch comprising:

input lines which are grouped into a plurality of groups;

means which compares time information added to cells within said group; and

selection means which selects a cell with the earliest time information according to the comparison,

wherein an input line of said selection means of an ith stage in said basic switch is an output line of said selection means of an (i-1)th stage where i is a natural number.

13. The ATM switch as claimed in claim 12, wherein a plurality of switches are provided in parallel, said switch including said basic switch.

14. The ATM switch as claimed in claim 13, further comprising:

splitting means which splits a cell into a

plurality of short cells;

means which transfers said short cells to said switches;

assembling means which assembles said short cells into said cell;

means which adds first time information to an arriving cell;

means which adds second time information to short cells obtained by splitting said arriving cell;

means which ensures a sequence of said short cells in said switch according to said first time information; and

means which ensures a sequence of said short cells in said assembling means according to said second time information.

15. The ATM switch as claimed in claim 14, wherein said splitting means splits a payload of a cell into a plurality of payloads, and rewrites the overhead of each payload.

16. An ATM switch comprising:

splitting means which splits a cell into a plurality of short cells;

a plurality of switches which transfer said short cells in parallel;

assembling means which assembles said short cells into said cell;

counting means which counts the number of output short cells being output from each of said

switches; and

first comparing means which compares bit information of a plurality of said output short cells which have the same value counted by said counting means,

wherein said assembling means includes means which assembles said short cells with the same bit information according to the comparison of said first comparing means.

17. The ATM switch as claimed in claim 16, wherein said switch includes at least one basic switch, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

18. The ATM switch as claimed in claim 16, comprising:

obtaining means which obtains an inferred delay time t instead of said counting means;

second comparing means which compares bit information of said short cells which are output from said switches, said short cells having delay time of $t \pm \tau$, τ being an acceptable fluctuation time.

19. The ATM switch as claimed in claim 18, wherein said obtaining means includes means which

obtains said inferred delay time t by comparing an input time of a short cell which is input to said switch with an output time of said short cell which is output from said switch.

20. An ATM switch which includes at least one basic switch, said basic switch comprising output buffer parts for each output line,

wherein said output buffer part comprises output buffers for each input line and a time sorting part which is connected to said output buffers, and

wherein said time sorting part outputs a head cell with the earliest time information among head cells stored in said each output buffer.

21. The ATM switch as claimed in claim 20, wherein said basic switch comprises:

address filters in front of said each output buffer,

wherein said address filter stores a cell arriving from said input line as an actual cell if the destination of said cell is an output line corresponding to said address filter, and

wherein said address filter stores a cell as a dummy cell after extracting time information of said cell if the destination of said cell is not an output line corresponding to said address filter.

22. The ATM switch as claimed in claim 20, wherein said basic switch, when a dummy cell arrives, stores said dummy cell in all output buffers.

23. The ATM switch as claimed in claim 20, further comprising adding means which adds time information to a cell, wherein said adding means generates a dummy cell if there is no arriving cell.

24. An ATM switch which includes a plurality of stages, wherein said stages are connected and each of said stages includes a plurality of basic switches, said ATM switch comprising:

a cell distribution part in said basic switch of a first stage,

wherein said cell distribution part determines a route of a cell to be transferred such that loads of routes within said ATM switch are equalized.

25. The ATM switch as claimed in claim 24, wherein said cell distribution part, when a cell arrives, determines a destination group of said cell, refers to a cell distribution history table, and determines a route which has transferred a minimum number of cells within a fixed time period among

routes corresponding to said destination group in said cell distribution history table.

26. An ATM switch which includes a plurality of stages, wherein said stages are connected and each of said stages includes a plurality of basic switches, said ATM switch comprising:

means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information; and

a cell distribution part in said basic switch of a first stage,

wherein said cell distribution part determines a route of a cell to be transferred such that loads of routes within said ATM switch are equalized.

27. A cell switch which includes at least one basic switch, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

28. The cell switch as claimed in claim 27, said means comprising:

a cross-point at which an input line and

an output line are crossed;

a first buffer which stores a cell arriving from said input line;

a second buffer which stores a cell arriving from a cross-point; and

means which compares time information of a head cell in said first buffer with time information of a head cell in said second buffer and sends a head cell with earlier time information to a cross-point or said output port.

29. A large-sized cell switch which includes interconnected cell switches each of which cell switches includes at least one basic switch, said basic switch comprising means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information.

30. A cell switch which includes at least one basic switch, said basic switch comprising:

input lines which are grouped into a plurality of groups;

means which compares time information added to cells within said group; and

selection means which selects a cell with the earliest time information according to the comparison,

wherein an input line of said selection means of an ith stage in said basic switch is an output line of said selection means of an (i-1)th

stage where i is a natural number.

31. A cell switch comprising:

splitting means which splits a cell into a plurality of short cells;

a plurality of switches which transfer said short cells in parallel;

assembling means which assembles said short cells into said cell;

counting means which counts the number of output short cells being output from each of said switches; and

comparing means which compares bit information of a plurality of said output short cells which have the same value counted by said counting means,

wherein said assembling means includes means which assembles said short cells with the same bit information according to the comparison of said comparing means.

32. A cell switch which includes at least one basic switch, said basic switch comprising output buffer parts for each output line,

wherein said output buffer part comprises output buffers for each input line and a time sorting part which is connected to said output buffers, and

wherein said time sorting part outputs a head cell with the earliest time information among head cells stored in said each output buffer.

33. A cell switch which includes a plurality of stages, wherein said stages are connected and each of said stages includes a plurality of basic switches, said cell switch comprising:

a cell distribution part in said basic switch of a first stage,

wherein said cell distribution part determines a route of a cell to be transferred such that loads of routes within said cell switch are equalized.

34. A cell switch which includes a plurality of stages, wherein said stages are connected and each of said stages includes a plurality of basic switches, said cell switch comprising:

means which refers to time information written in a header of an input cell and switches cells to an output port in an ascending order of said time information; and

a cell distribution part in said basic switch of a first stage,

wherein said cell distribution part determines a route of a cell to be transferred such that loads of routes within said cell switch are equalized.

35. A basic switch which inputs a cell, and outputs said cell to an output port on the basis of header information of said cell, said basic switch comprising means which refers to time information written in a header of said cell and switches cells to said output ports in an ascending order of said time information.

36. The basic switch as claimed in claim 35, said means comprising:

a cross-point at which an input line and an output line are crossed;

a first buffer which stores a cell arriving from said input line;

a second buffer which stores a cell arriving from a cross-point; and

means which compares time information of a head cell in said first buffer with time information of a head cell in said second buffer and sends a head cell with earlier time information to a cross-point or said output port.

37. A basic switch which inputs a cell, and outputs said cell to an output port on the basis of header information of said cell, said basic switch comprising:

input lines which are grouped into a plurality of groups;

means which compares time information added to cells within said group; and

selection means which selects a cell with the earliest time information according to the comparison,

wherein an input line of said selection means of an ith stage in said basic switch is an output line of said selection means of an (i-1)th stage where i is a natural number.

38. A basic switch which inputs a cell, and outputs said cell to an output port on the basis of header information of said cell, said basic switch comprising output buffer parts for each output line,

wherein said output buffer part comprises output buffers for each input line and a time sorting part which is connected to said output buffers, and

wherein said time sorting part outputs a head cell with the earliest time information among head cells stored in said each output buffer.

39. The basic switch as claimed in claim 38, wherein said basic switch comprises:

address filters in front of said each output buffer,

wherein said address filter stores a cell arriving from said input line as an actual cell if the destination of said cell is an output line corresponding to said address filter, and

wherein said address filter stores a cell as a dummy cell after extracting time information of

said cell if the destination of said cell is not an output line corresponding to said address filter.

40. The basic switch as claimed in claim 38, wherein said basic switch, when a dummy cell arrives, stores said dummy cell in all output buffers.